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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,049	09/04/2003	Patrick Lampin	FR920020057	2048

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EXAMINER	
SINKANTARAKORN, PAWARIS	
ART UNIT	**PAPER NUMBER**
2616	

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09/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/605,049	LAMPIN ET AL.	
	Examiner	Art Unit	
	Pao Sinkantarakorn	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 are pending. Claims 3-6 are newly added.

Claim Rejections - 35 USC § 103

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Nguyen et al. (US 7042895).

Regarding claims 1 and 6, the admitted prior art discloses in a telecommunication system split into a plurality of subsystems adapted to exchange serial data bits arranged in frames n bits long n-bit frames according to a dynamic time division multiplexing (TDM) access method wherein the time is split in time slots, so that to each bit position (Bit1 to Bitn) of the frame is associated either one among N logical channels or a null value, N being the maximum number of logical channels that can be simultaneously opened and wherein to each logical channel (X) is associated an identifier (LC X) coded on p bits where N, n, and p are integers, wherein the improvement comprises:

first data storage means comprising an nxp memory block to store the time slot assignment (TSA) table which specifies for each bit position of the n-bit frame, the logical channel it belongs to at a given time, describing thereby the different time slots (see paragraph 4, lines 9 – 16);

input bus means for inputting the logical channel identifiers into the first data storage means from a computer or an application software (see paragraph 7, lines 7 – 8);

logic circuit means connected to the first and second data storage means that enables or disables the transmission of the logical channel identifiers to an output bus means for subsequent processing by a time slot assignor (see paragraph 6, lines 15 –

20, wherein memory blocks 21-1 and 21-2 correspond to first and second data storage means respectively, multiplexer corresponds to logic circuit means);

The admitted prior art fails to teach second data storage means comprising a Nxl register to store status bits that indicates for each logical channel its status, "assigned" when it has a first value or "unassigned" when it has another value;

Nguyen et al. from the same or similar field of endeavors teach second data storage means comprising a Nxl register to store status bits that indicates for each logical channel its status, "assigned" when it has a first value or "unassigned" when it has another value (see column 4, lines 50 – 52, 63 – 67, column 5, lines 1 – 3, 48 - 55);

Thus, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use second data storage means comprising a Nxl register to store status bits that indicates for each logical channel its status, "assigned" when it has a first value or "unassigned" when it has another value in the method system taught by the admitted prior art in order to allow better system performance by reducing the demand on processor (see column 5, lines 21 – 23).

The admitted prior art fail to teach input bus means for inputting the value of the status bits in the second data storage means from a computer.

Nguyen et al. from the same or similar field of endeavors teach input bus means for inputting the value of the status bits in the second data storage means from a computer (see column 5, lines 22 – 35).

Thus, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use input bus means for inputting the value of the status bits in the second data storage means from a computer in order to allow accurate channel status record keeping (see column 5, lines 23 – 25).

The admitted prior art fail to teach logic circuit means connected to the first and second data storage means that enables or disables the transmission of the logical channel identifiers depending upon they are "assigned" or "unassigned".

Nguyen et al. from the same or similar field of endeavors teach logic circuit means connected to the first and second data storage means that enables or disables the transmission of the logical channel identifiers depending upon they are "assigned" or "unassigned" (see column 6, lines 45 – 55, wherein the tri-state buffer corresponds to logic circuit means).

Thus, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use logic circuit means connected to the first and second data storage means that enables or disables the transmission of the logical channel identifiers depending upon they are "assigned" or "unassigned" in the system taught by the admitted prior art in order to allow efficient bus access control by using only one shift register and storage register (see column 6, lines 50 – 53);

regarding claim 2, the admitted prior art disclose the null value corresponds to a bit position to which none logical channel is assigned (see paragraph 6, lines 6 – 8);

regarding claim 3, the admitted prior art discloses the logic circuit means comprises p parallel two-way AND gates (see figure 2 reference numeral 25).

Regarding claim 4, the admitted prior art discloses the AND gates receive inputs from the memory block. The admitted prior art does not disclose the gates receive an input from the register.

Nguyen et al. from the same or similar fields of endeavors teach a system, wherein a logic gate receives an input from a register (see figure 4 reference numeral 42, 46, and 46A).

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to implement a register as taught by Nguyen et al. into the conventional dynamic time division multiplexing circuit of the admitted prior art in order to allow efficient bus access control by using only one shift register and storage register (see column 6, lines 50 – 53).

Regarding claim 5, the admitted prior art discloses each AND gate receives one of p bits from a channel identifier data entry in the TSA table (see paragraph 6 lines 1-4 and 15-18, the TSA table is stored in memory block 21-1 and the memory block 21-1 is connected to an AND gate 25).

Response to Arguments

6. Applicant's arguments filed 7/3/2007 have been fully considered but they are not persuasive.

7. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the teaching, suggestion, or motivation found in the knowledge generally available to one of ordinary skill in the art to combine the teachings of Nguyen et al. and the admitted prior art to produce the claimed invention is that it accommodates and maximizes efficiency for different TDM arrangements. *See KSR, 82 USPQ2d 1385 (2007)*. The combination of the shift register 42, which is loaded with data bits indicating the status of a channel, with the admitted prior art would result in the claimed invention. By replacing the memory block 21-2 of the admitted prior art with the shift register 42 of Nguyen et al., the TDM system is not converted to static TDM system in any way.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pao Sinkantarakorn whose telephone number is 571-

270-1424. The examiner can normally be reached on Monday-Thursday 9:00am-3:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PS

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER